## PATENT NUMBER and **ISSUE DATE**

## U.S. UTILITY Patent Application

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			layout method	thereof	U.S.DEPT. OF COMI	M./PAT.& TM-PTO-436L(Re	ev. 12-94)
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	** FOREIGN A JAPAN P 2001  PG-PUB DO N Foreign priority clai 35 USC 119 condit Veilfied and Ackno TITLE: Semico	**APPLICANTS: Hino You **APPLICANTS: Hino You **CONTINUING DATA VERIFIED **FOREIGN APPLICATIONS VE JAPAN P 2001-053627 02/28/200 PG-PUB DO NOT PUBLISH Foreign priority claimed 35 USC 119 conditions met Verified and Acknowledged Examiners's in	**APPLICANTS: Hino Yoshinori; Tarana Pulicants: Hino Yoshinori; Tarana Pulicantons Verified:  **FOREIGN APPLICATIONS VERIFIED: JAPAN P 2001-053627 02/28/2001  PG-PUB DO NOT PUBLISH Foreign priority claimed	***FOREIGN APPLICATIONS VERIFIED:  JAPAN P 2001-053627 02/28/2001  PG-PUB DO NOT PUBLISH Poreign priority claimed pyes no 35 USC 119 conditions met pyes no verified and Acknowledged Examiners's intials  TITLE: Semiconductor device and pattern layout method	***APPLICANTS: Hino Yoshinori; Takeishi Naoei; 2813  ***CONTINUING DATA VERIFIED:  JAPAN P 2001-053627 02/28/2001  PG-PUB DO NOT PUBLISH	**************************************	*** FOREIGN APPLICATIONS VERIFIED:  JAPAN P 2001-053627 02/28/2001  Foreign priority claimed 35 USC 119 conditions met  Verified and Acknowledged Examiners's initials  TITLE: Semiconductor device and pattern layout method thereof  U.S. OEPT. OF COMM./PATA 17N-PTO-JSBURG.

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		DISCLAMER	WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.						
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